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FIG. 1B
PRIOR ART

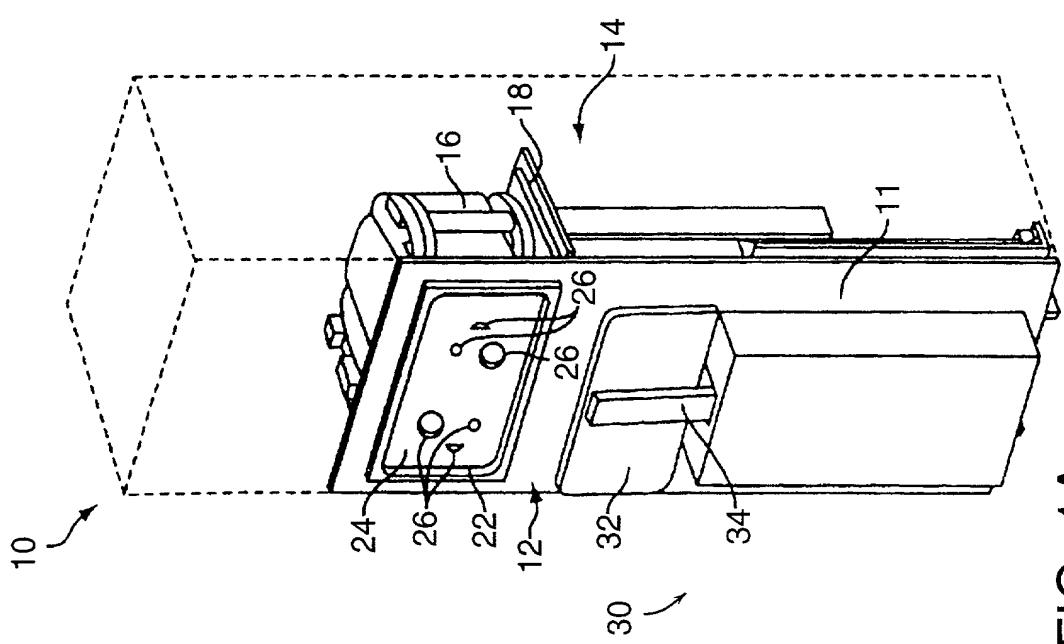
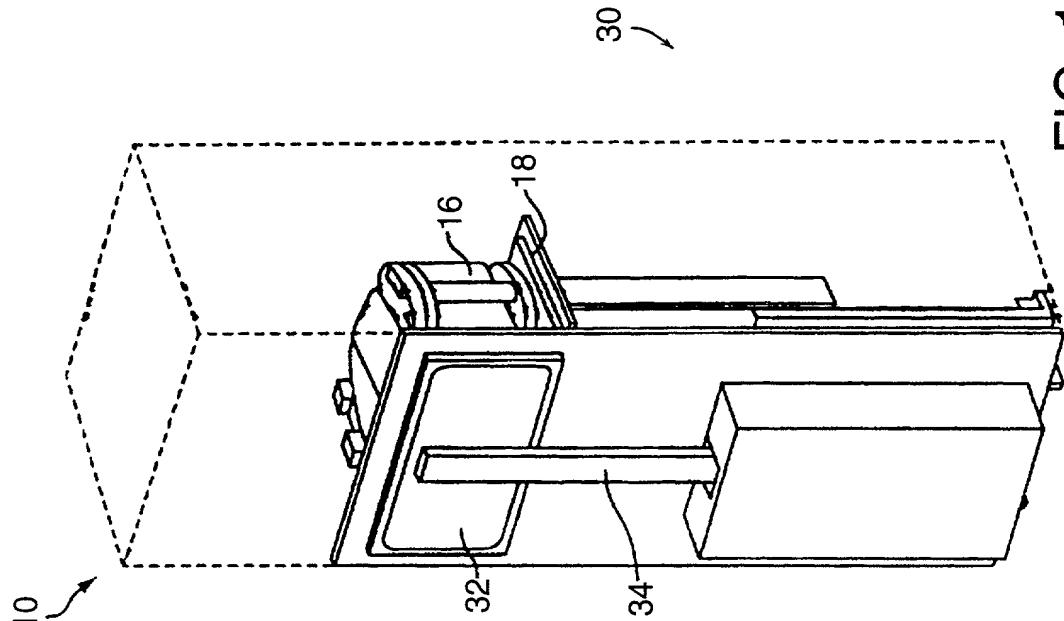


FIG. 1A
PRIOR ART

FIG. 1D
PRIOR ART

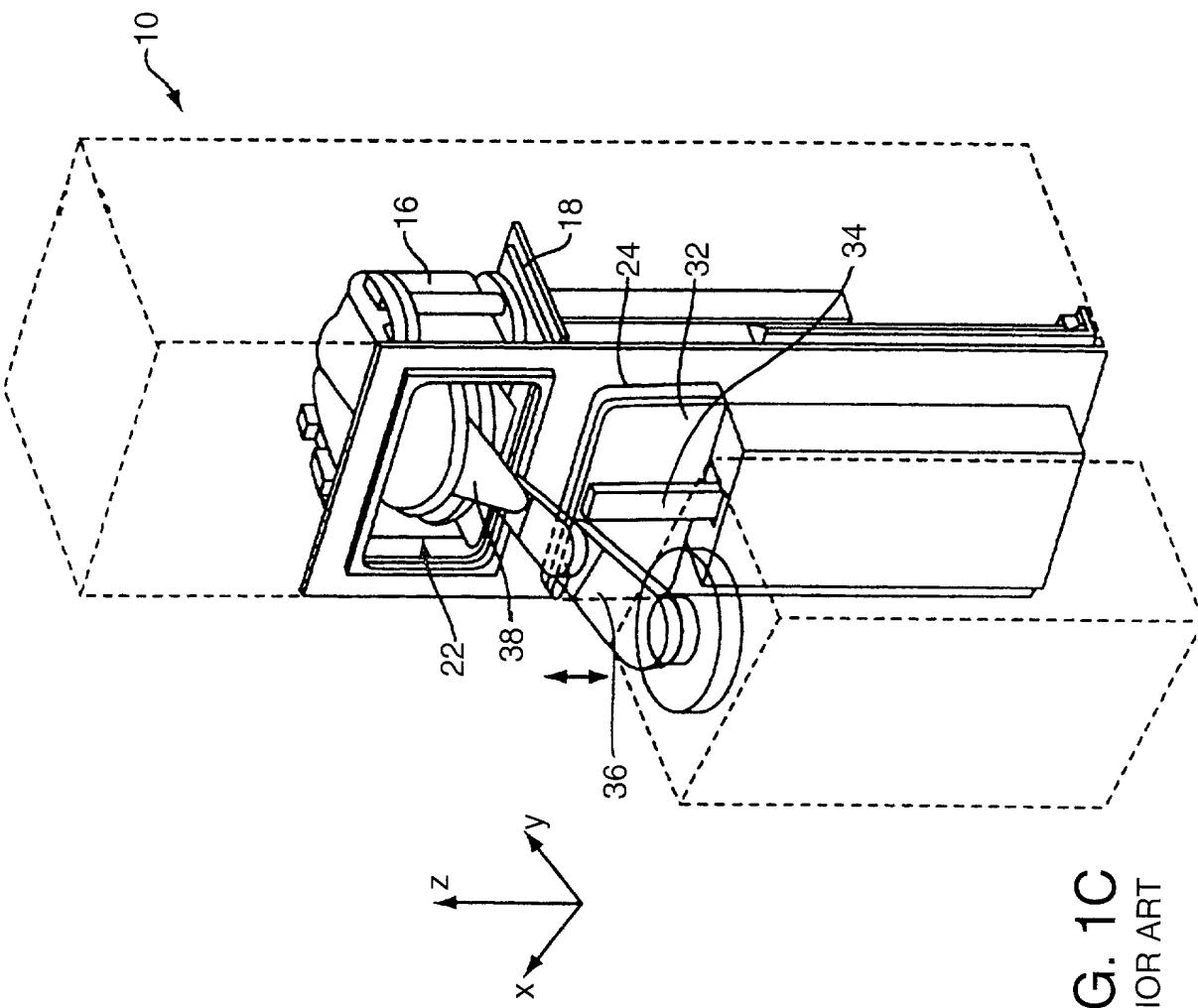
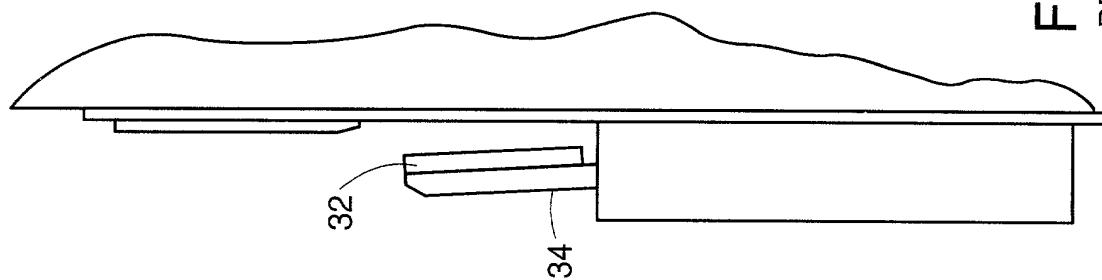


FIG. 1C
PRIOR ART

3/28

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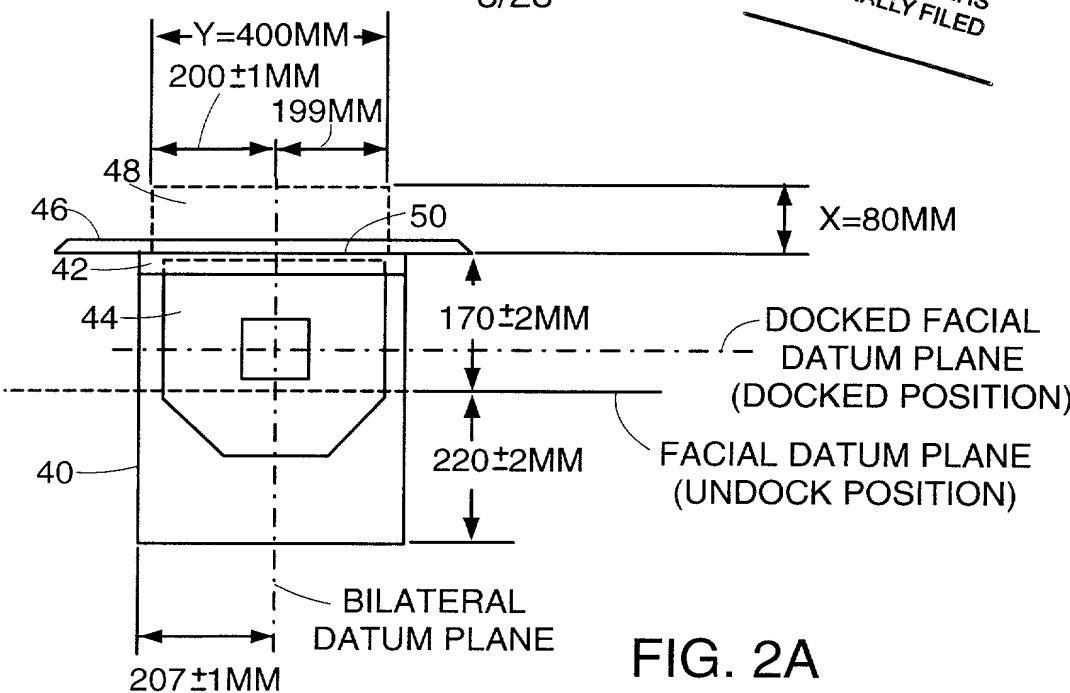


FIG. 2A

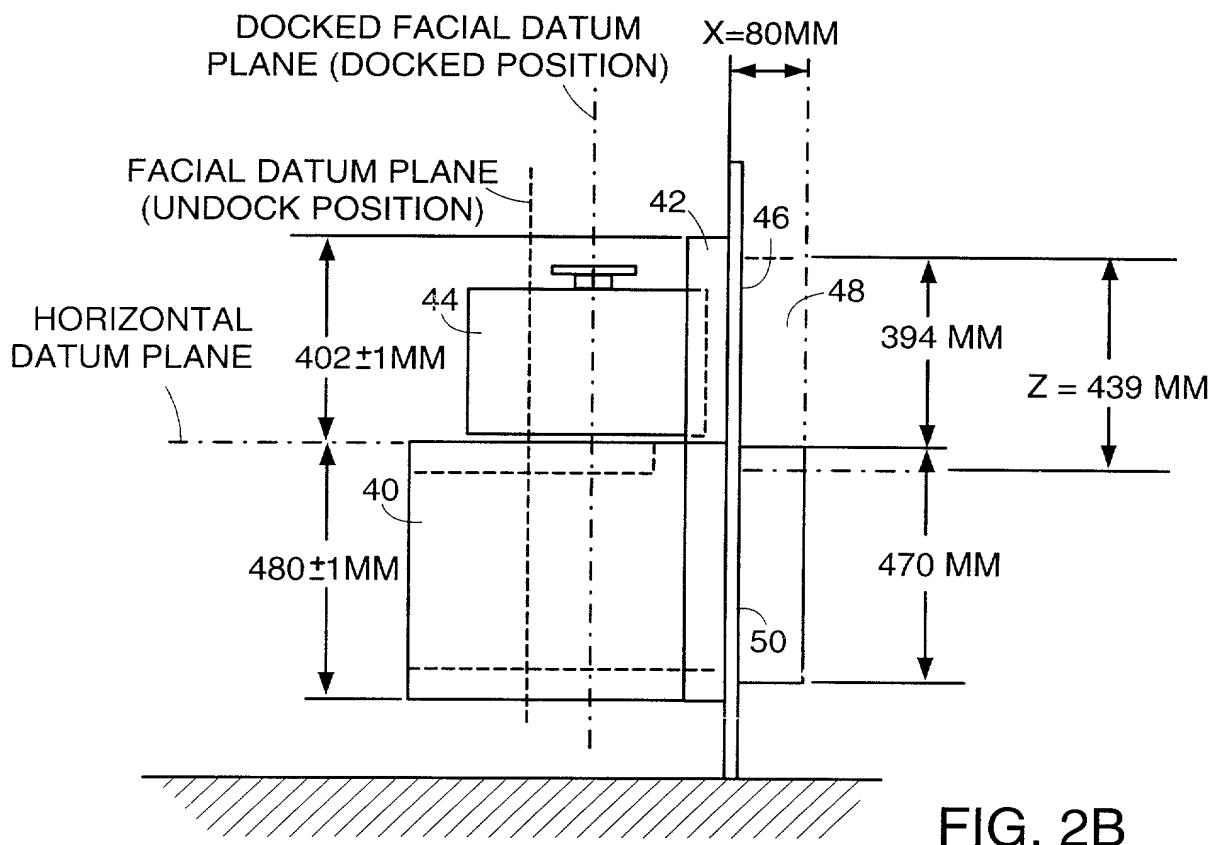


FIG. 2B

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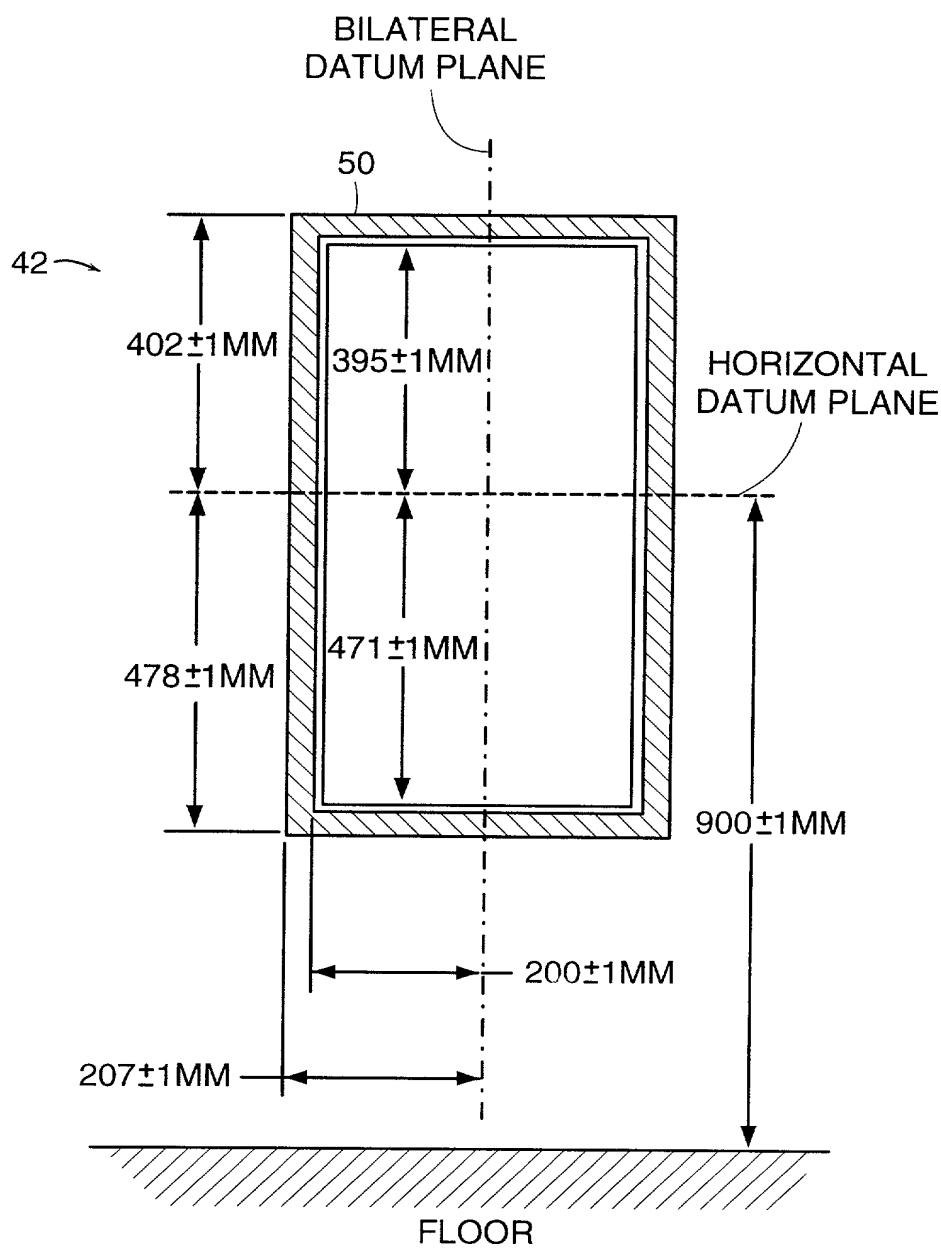
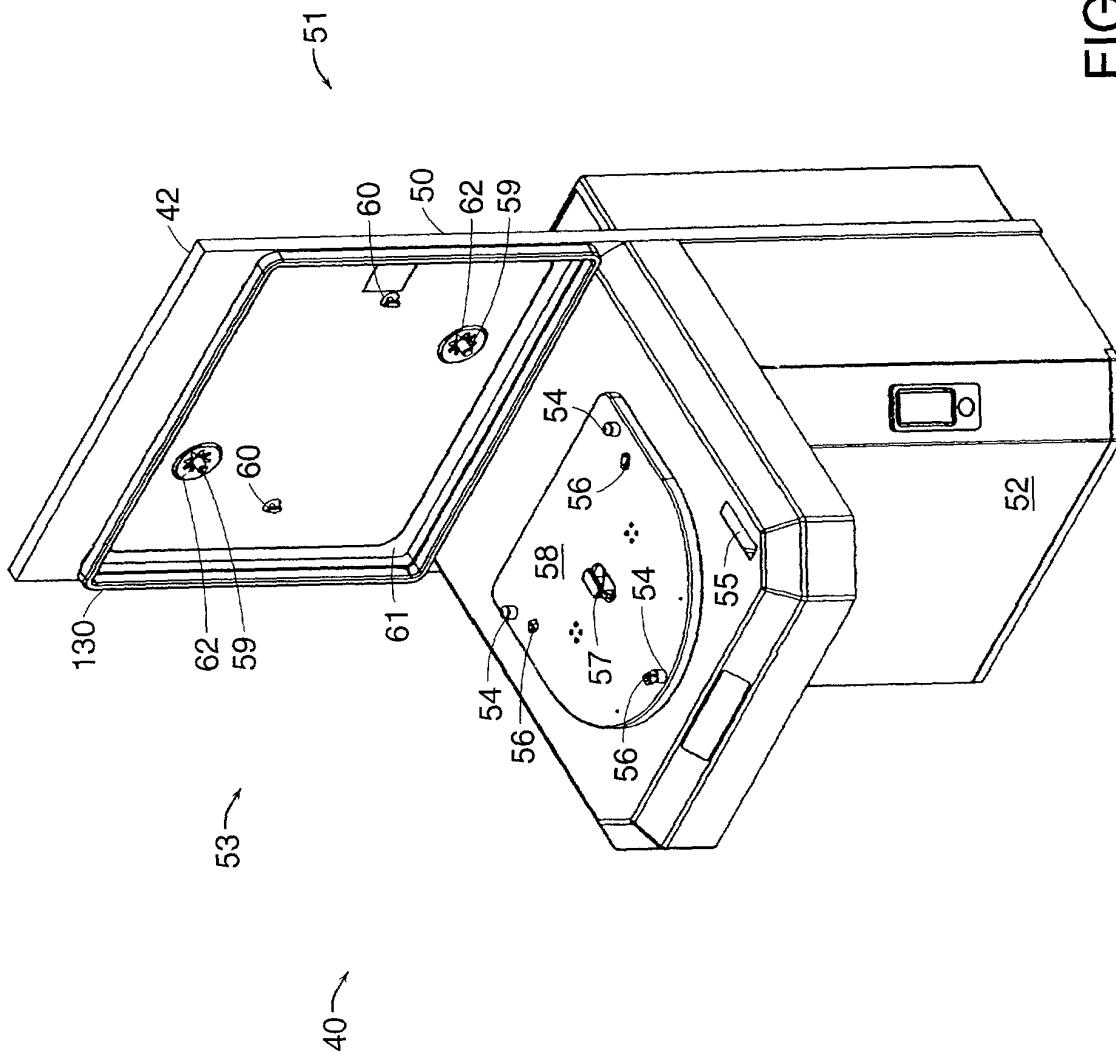


FIG. 2C

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FIG. 3

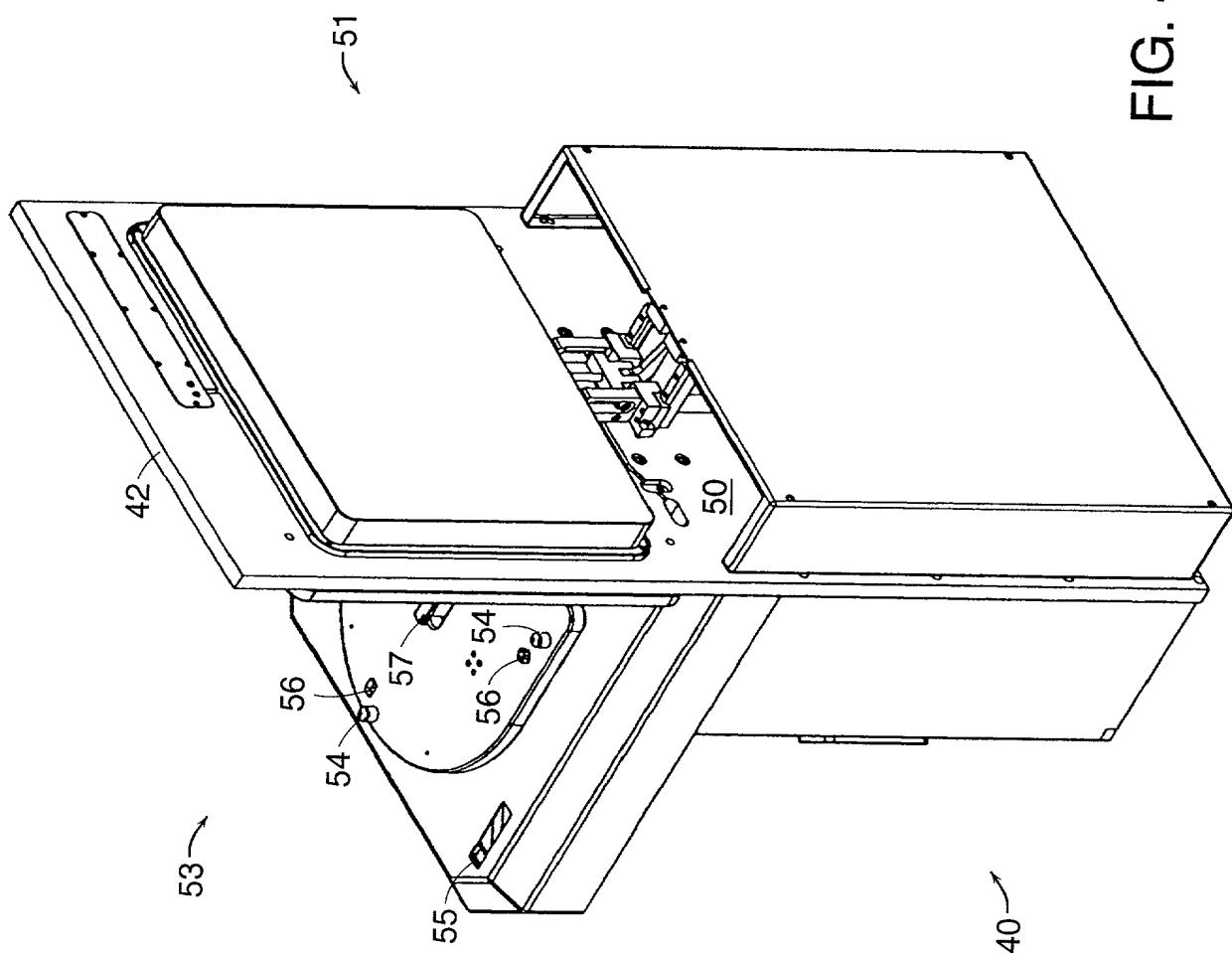


Title: Apparatus and Methods of Semiconductor
Wafer Processing Equipment
Inventor: Soucy et al.
Serial No. 09/897,820
Atty Docket No. APE-001
Atty: John V. Forcier

6/28

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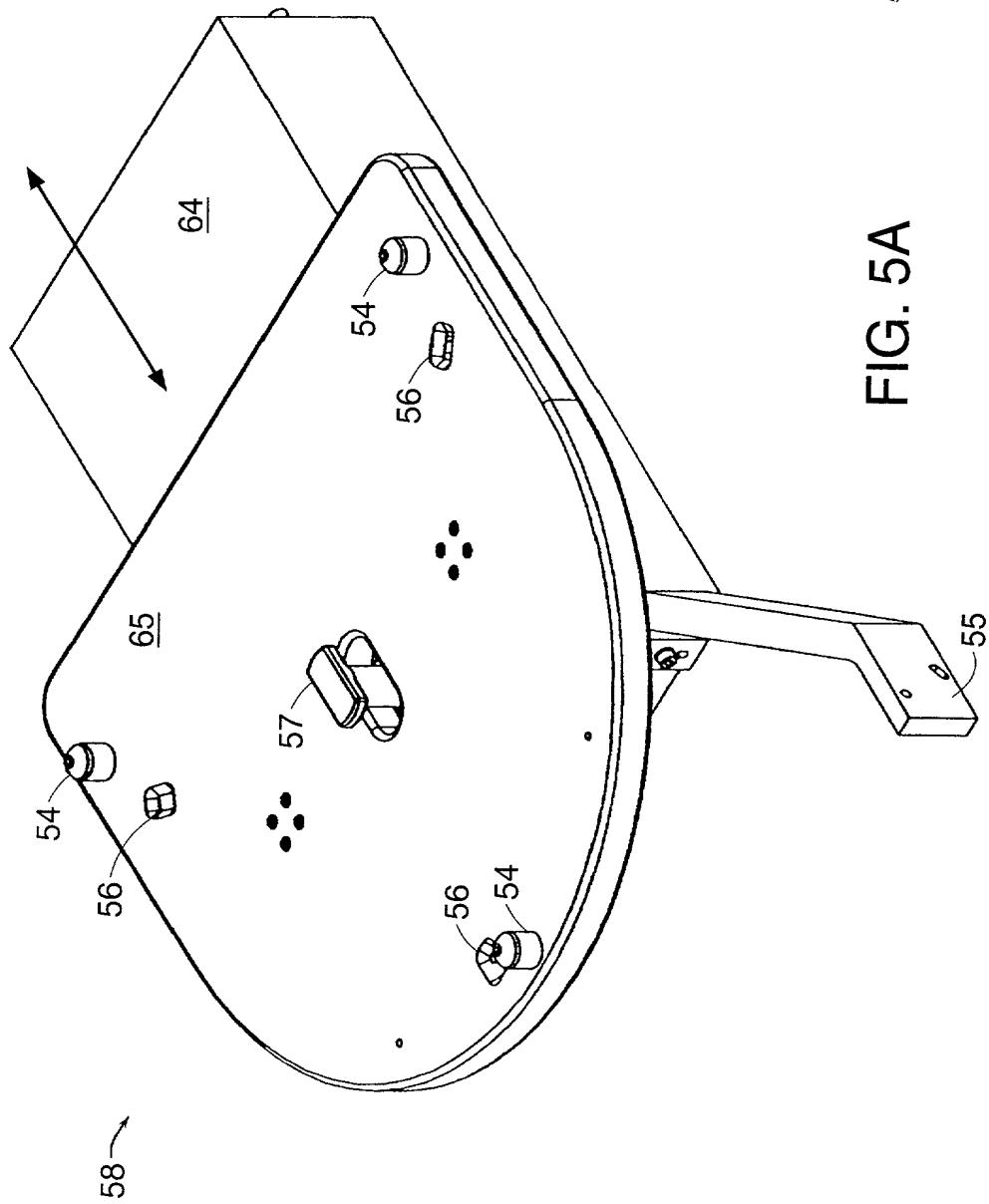
FIG. 4



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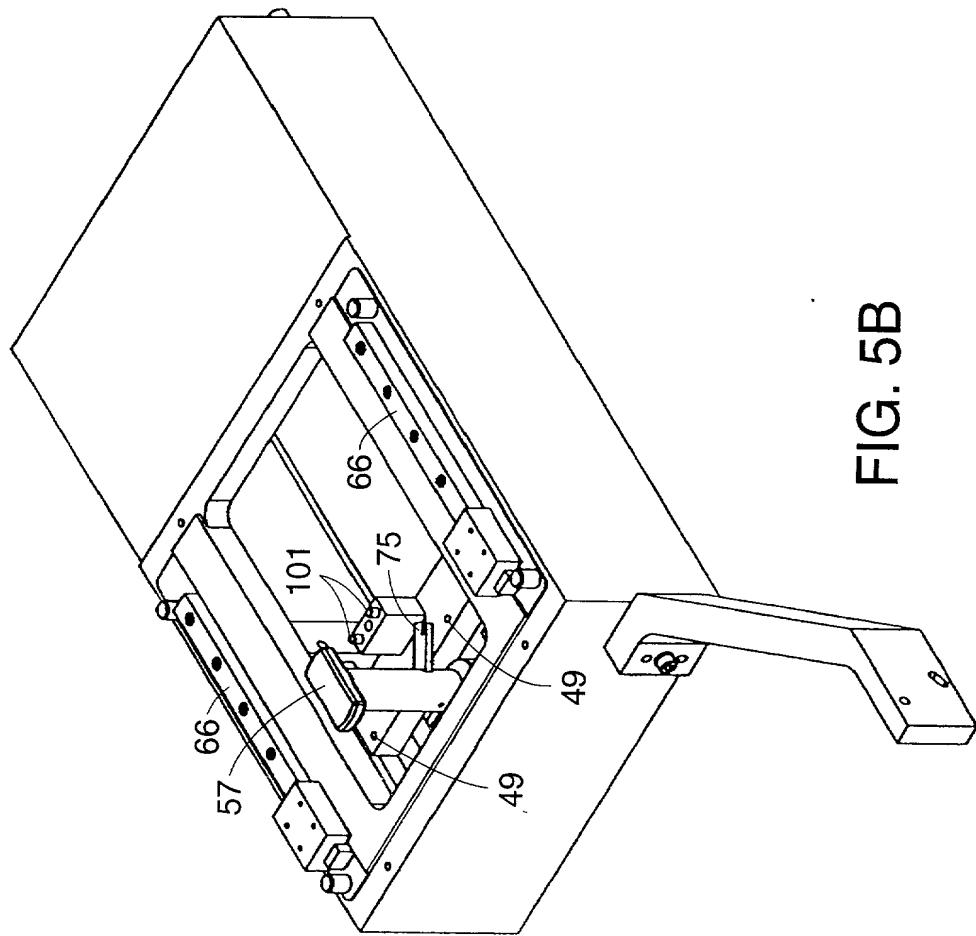


FIG. 5B

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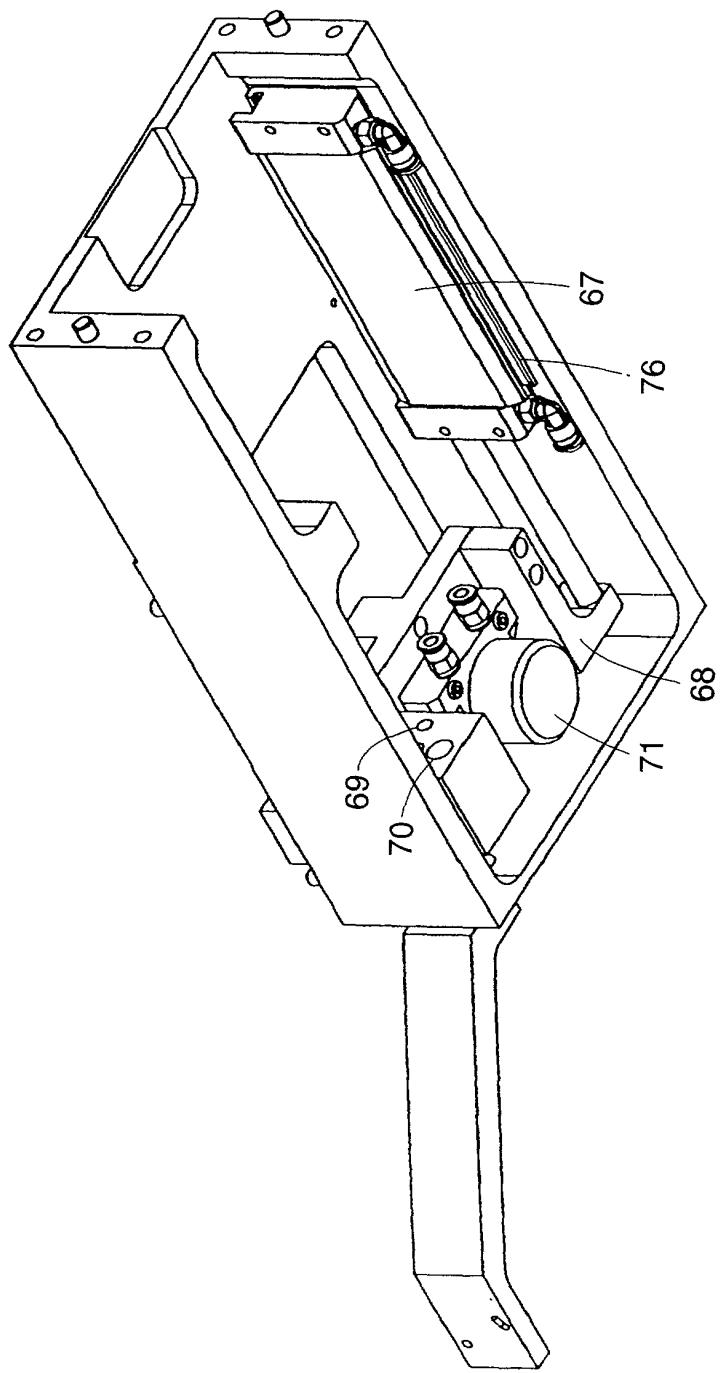


FIG. 5C

Title: Apparatus and Methods of Semiconductor
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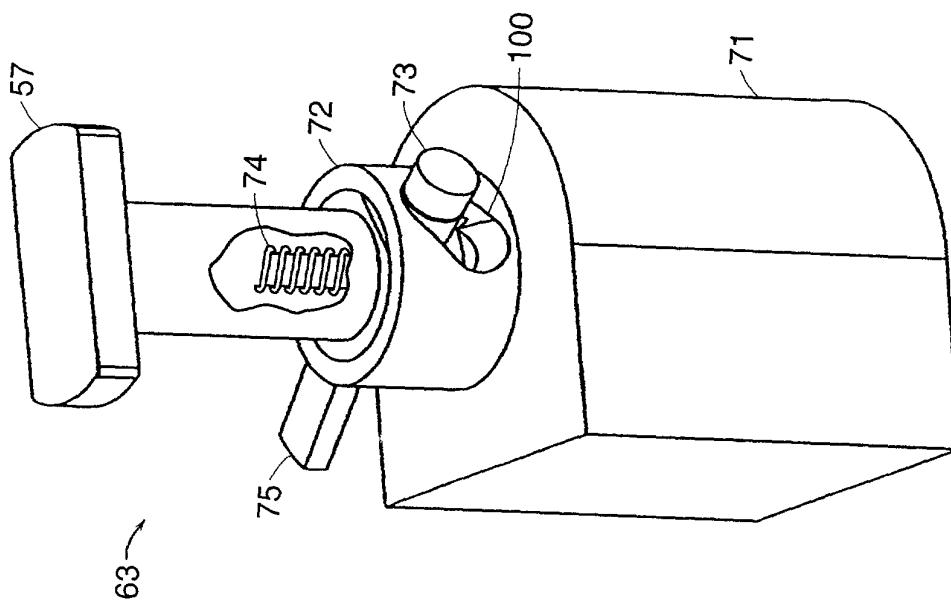


FIG. 5D

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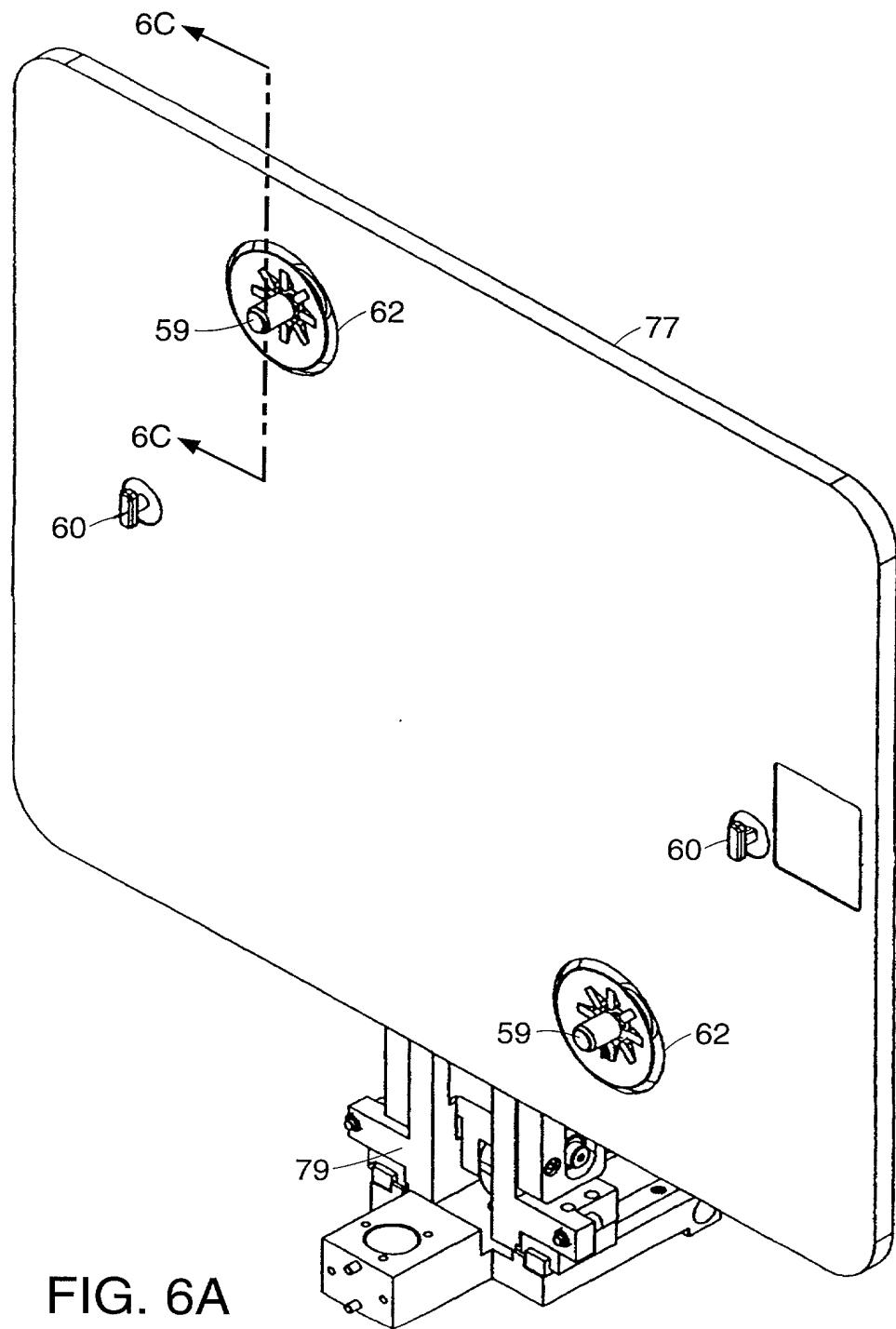


FIG. 6A

12/28

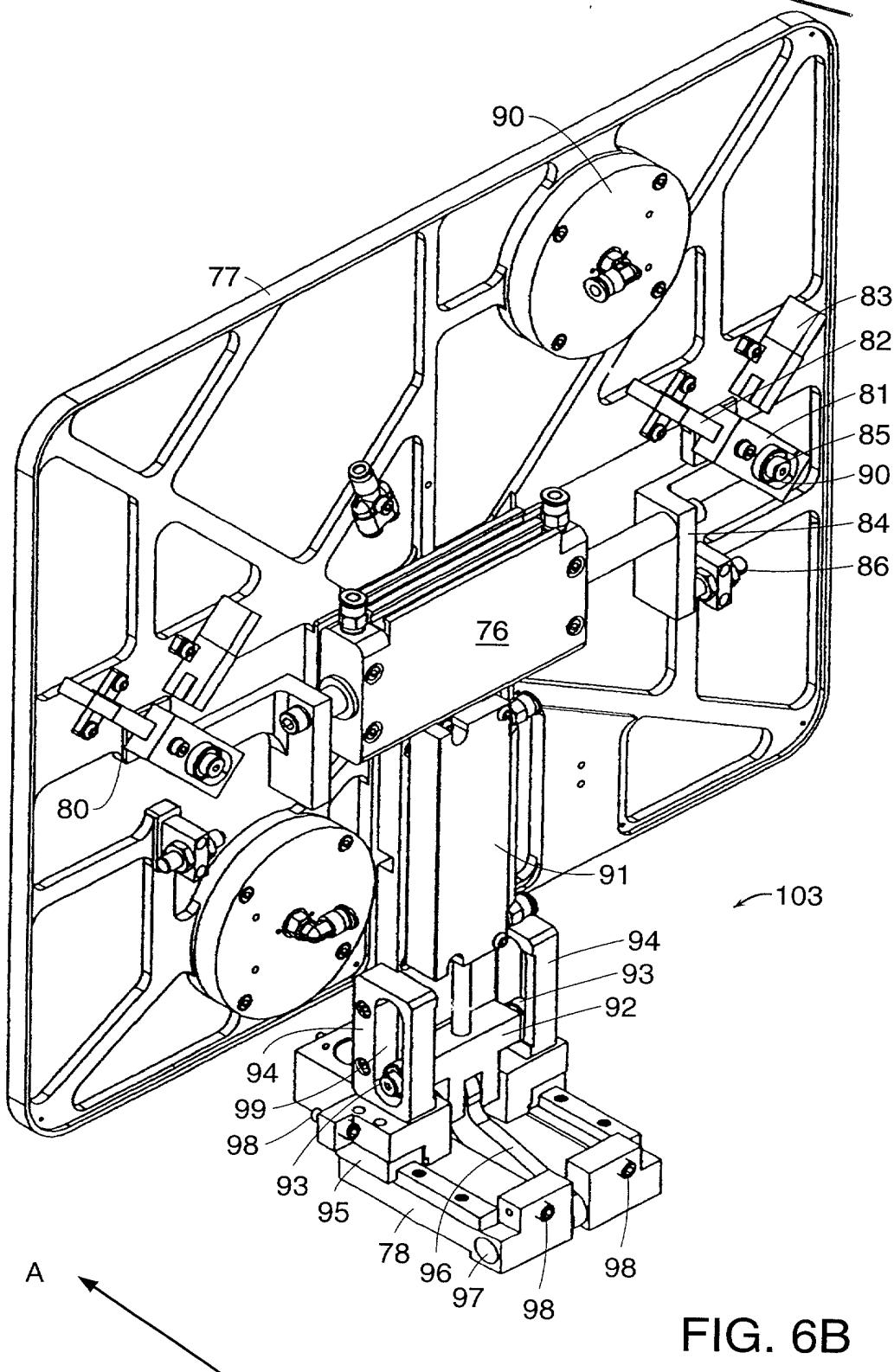


FIG. 6B

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13/28

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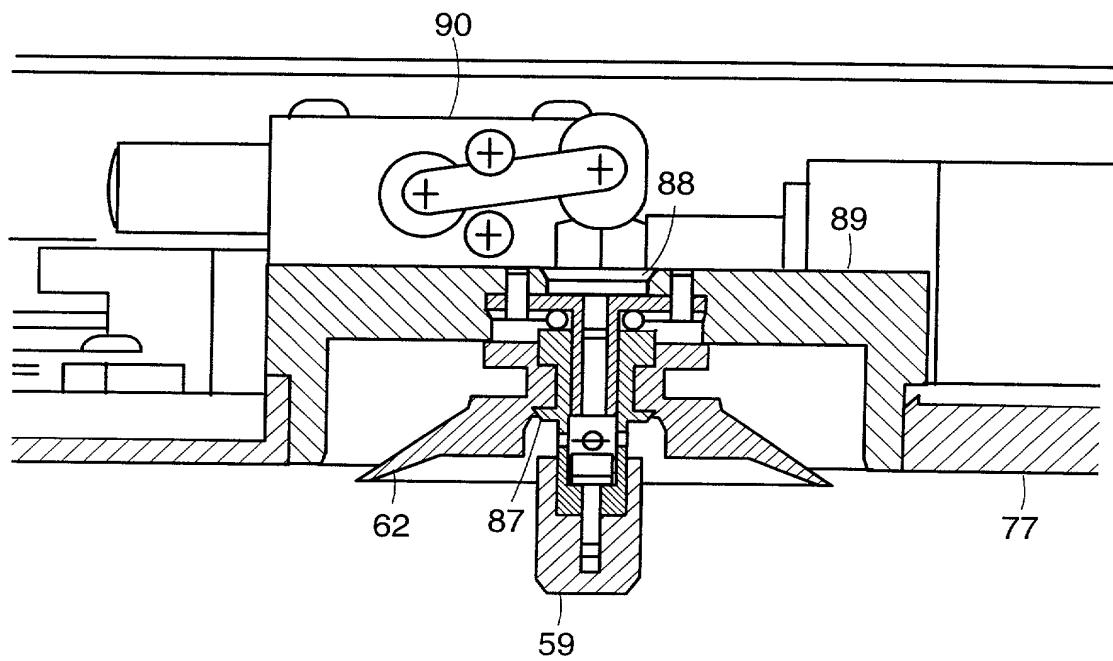


FIG. 6C

Title: Apparatus and Methods of Semiconductor
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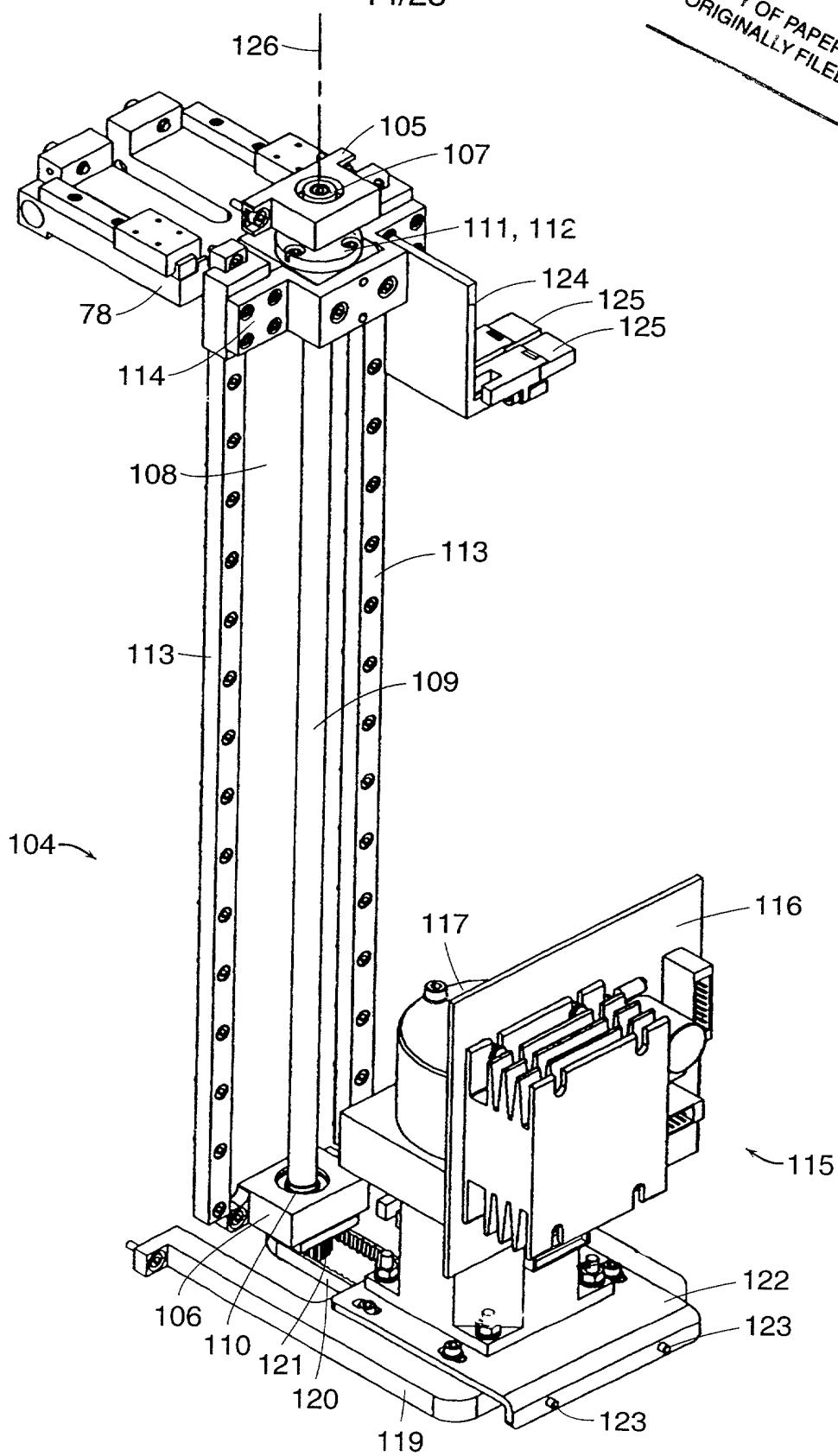


FIG. 7

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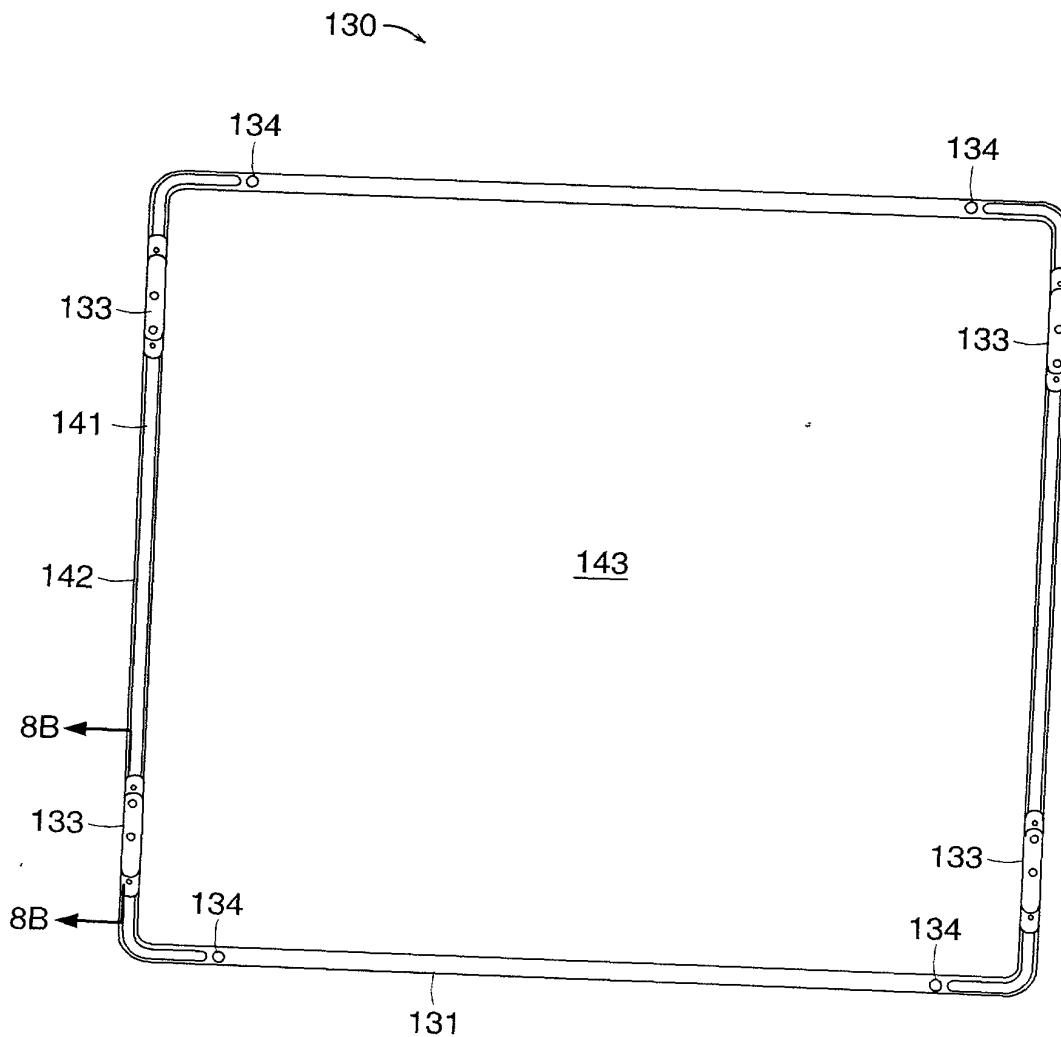


FIG. 8A

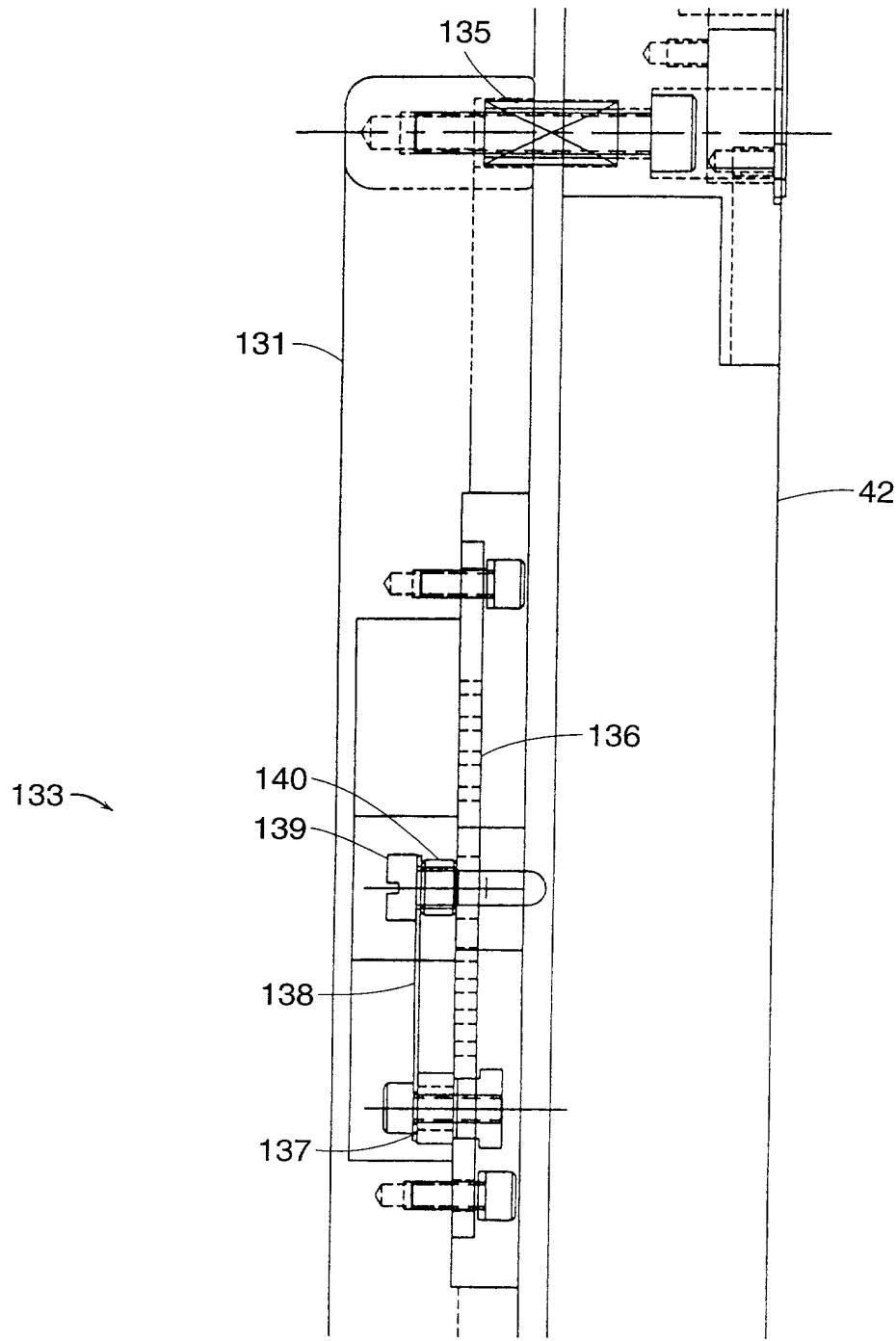


FIG. 8B

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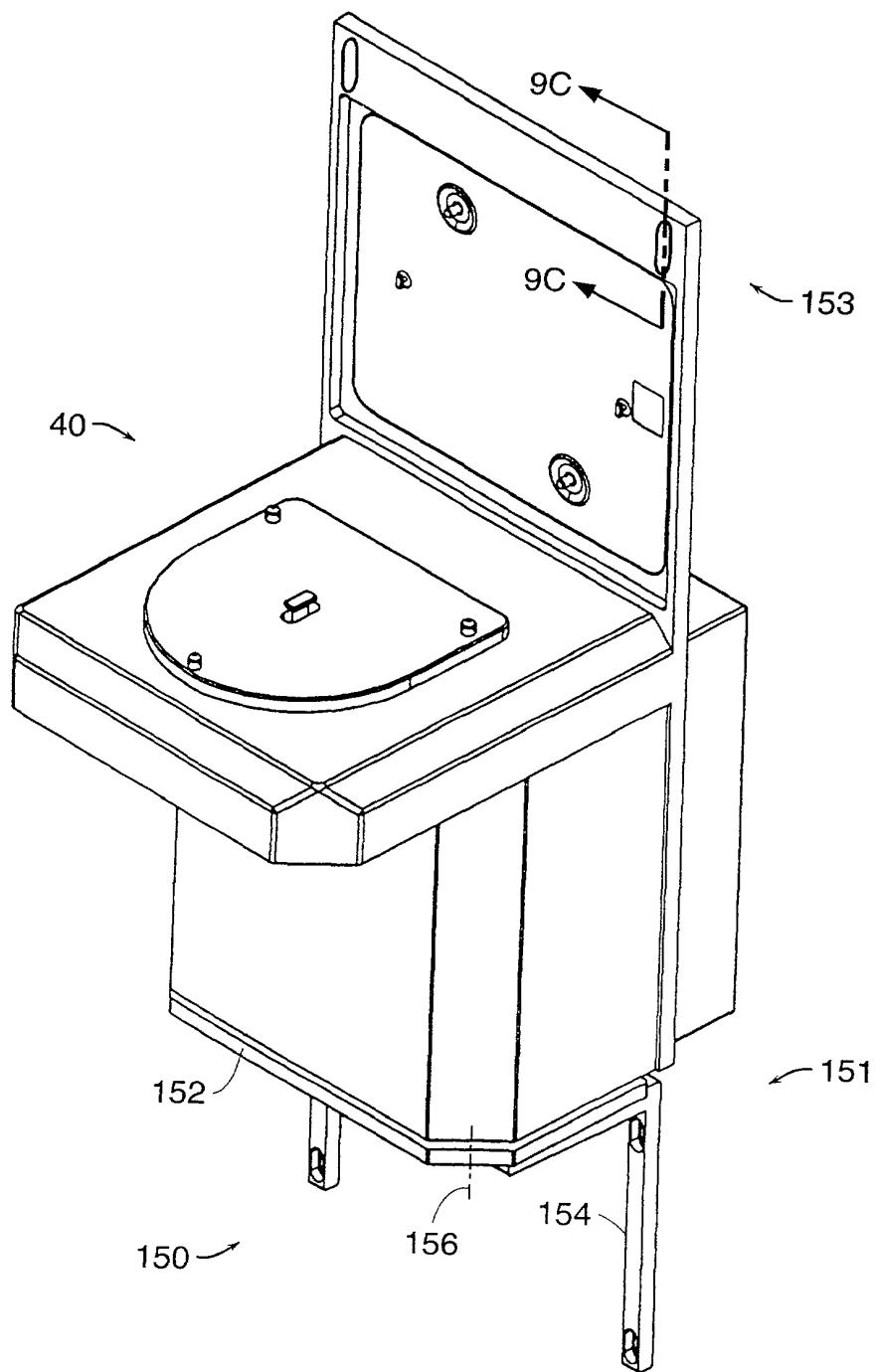


FIG. 9A

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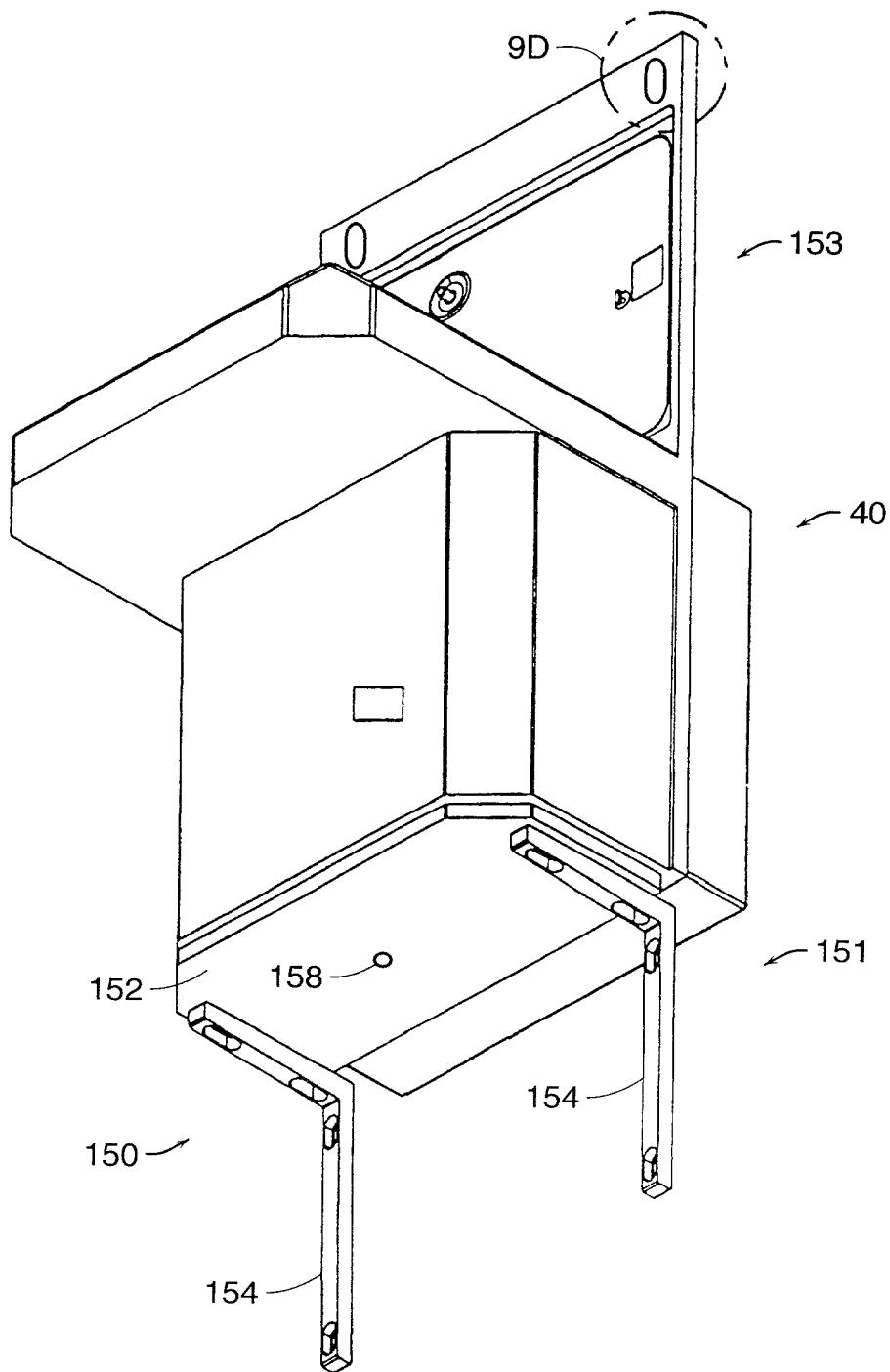


FIG. 9B

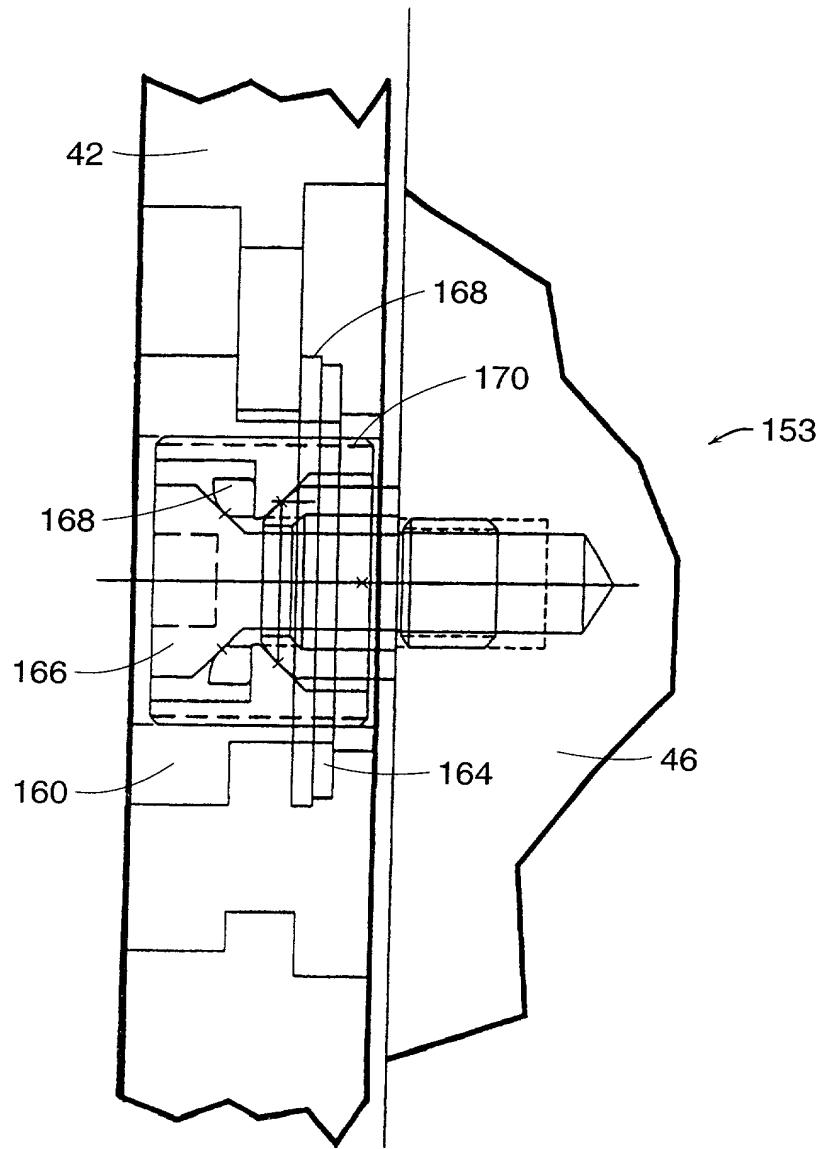


FIG. 9C

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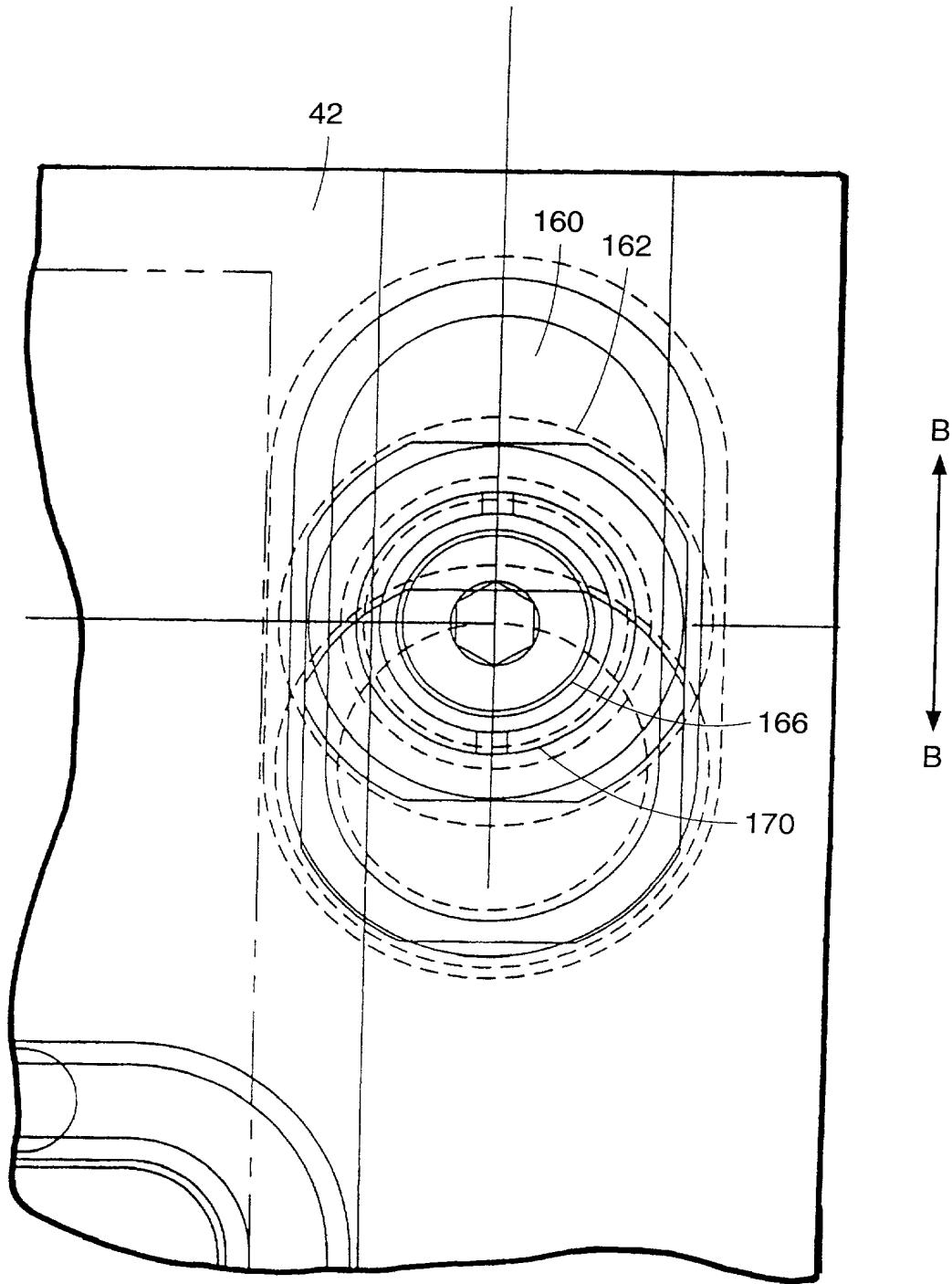


FIG. 9D

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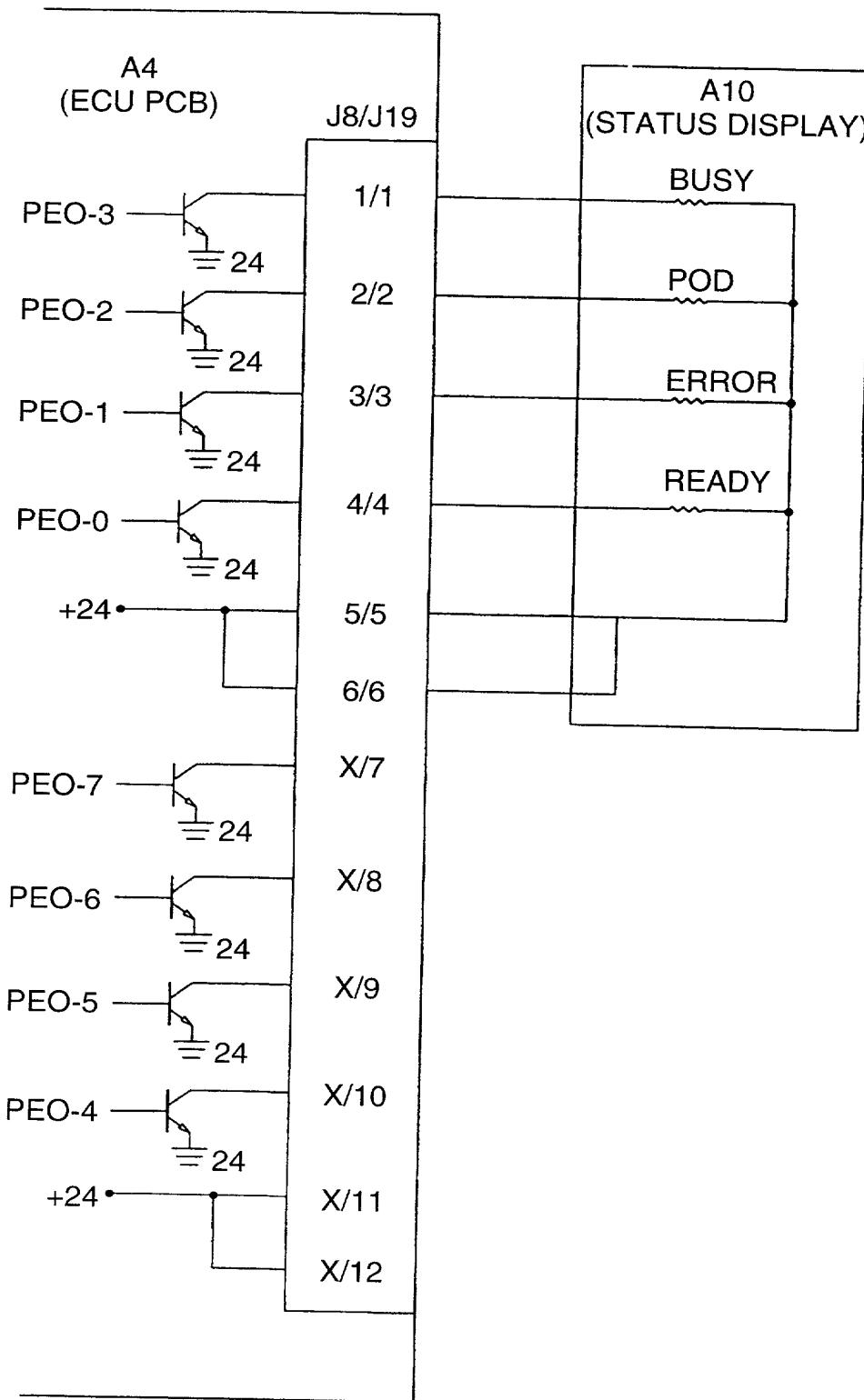


FIG. 10A

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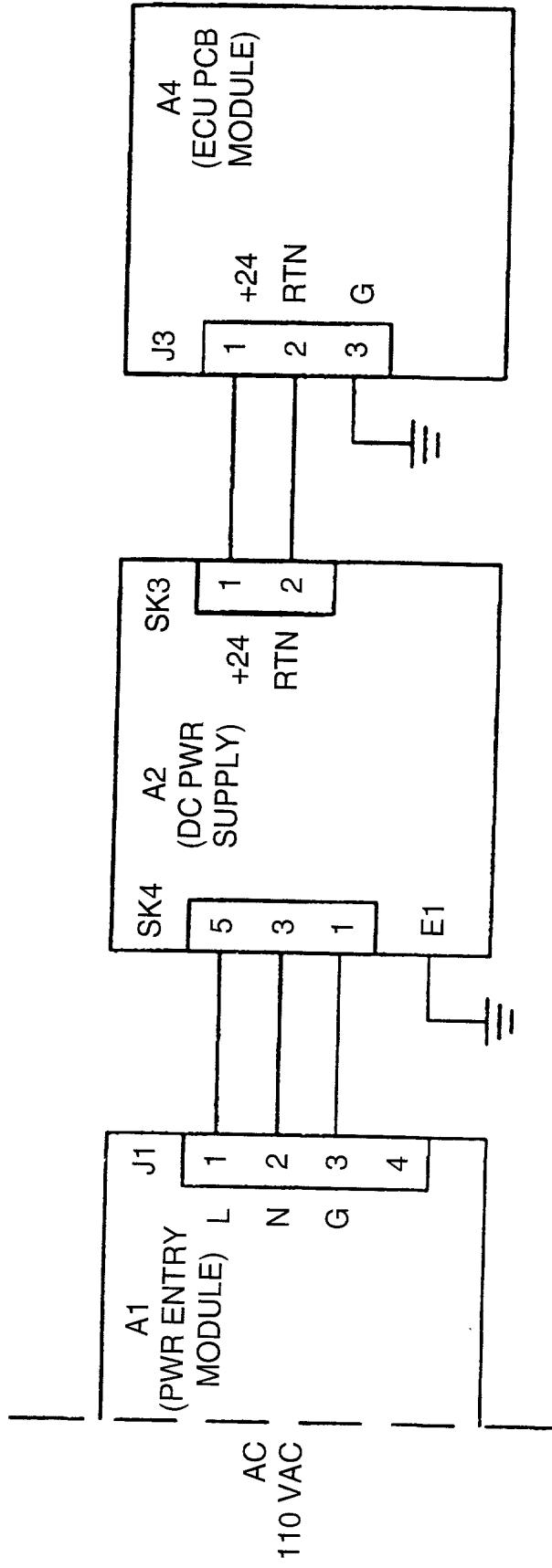


FIG. 10B

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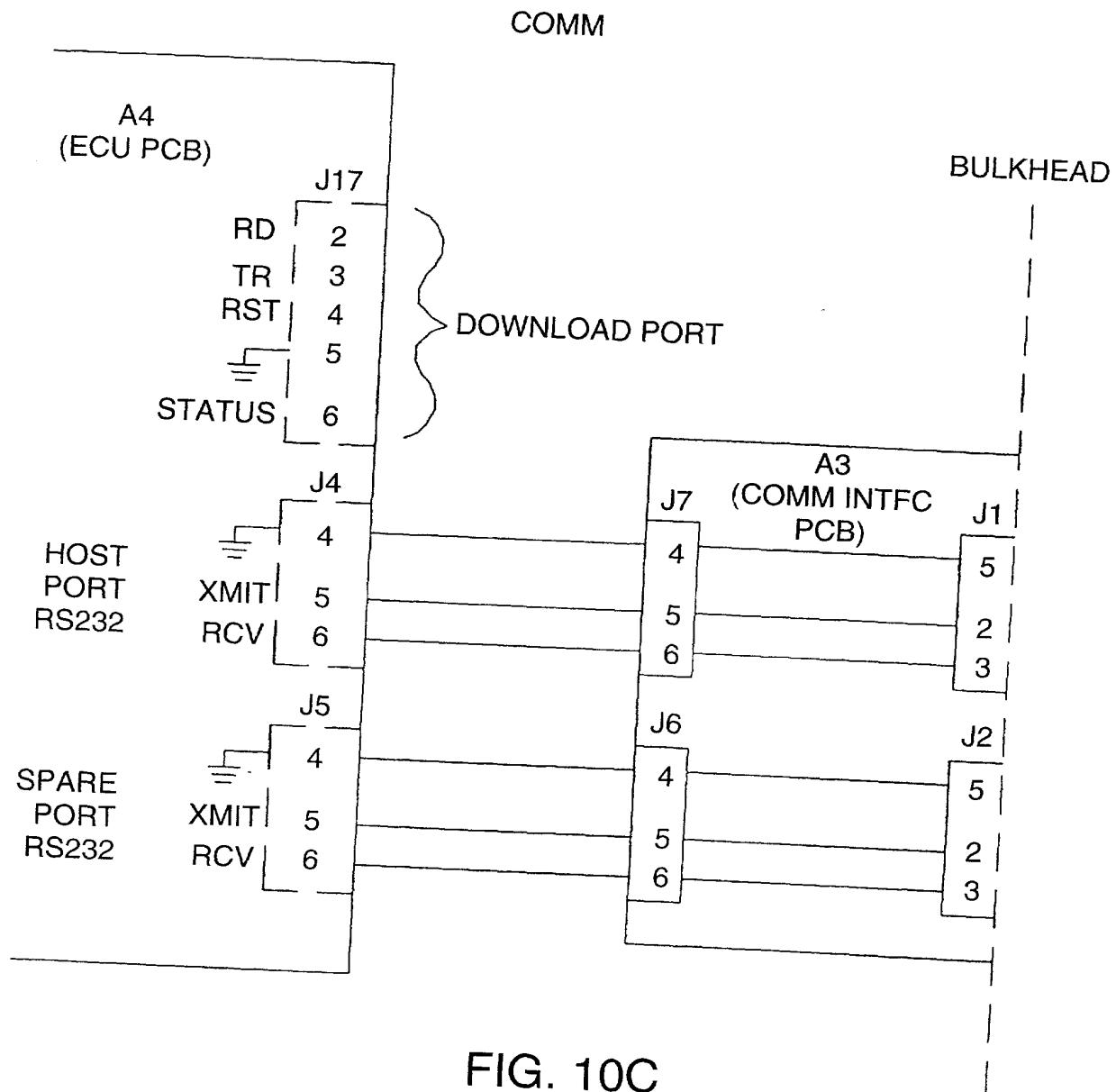


FIG. 10C

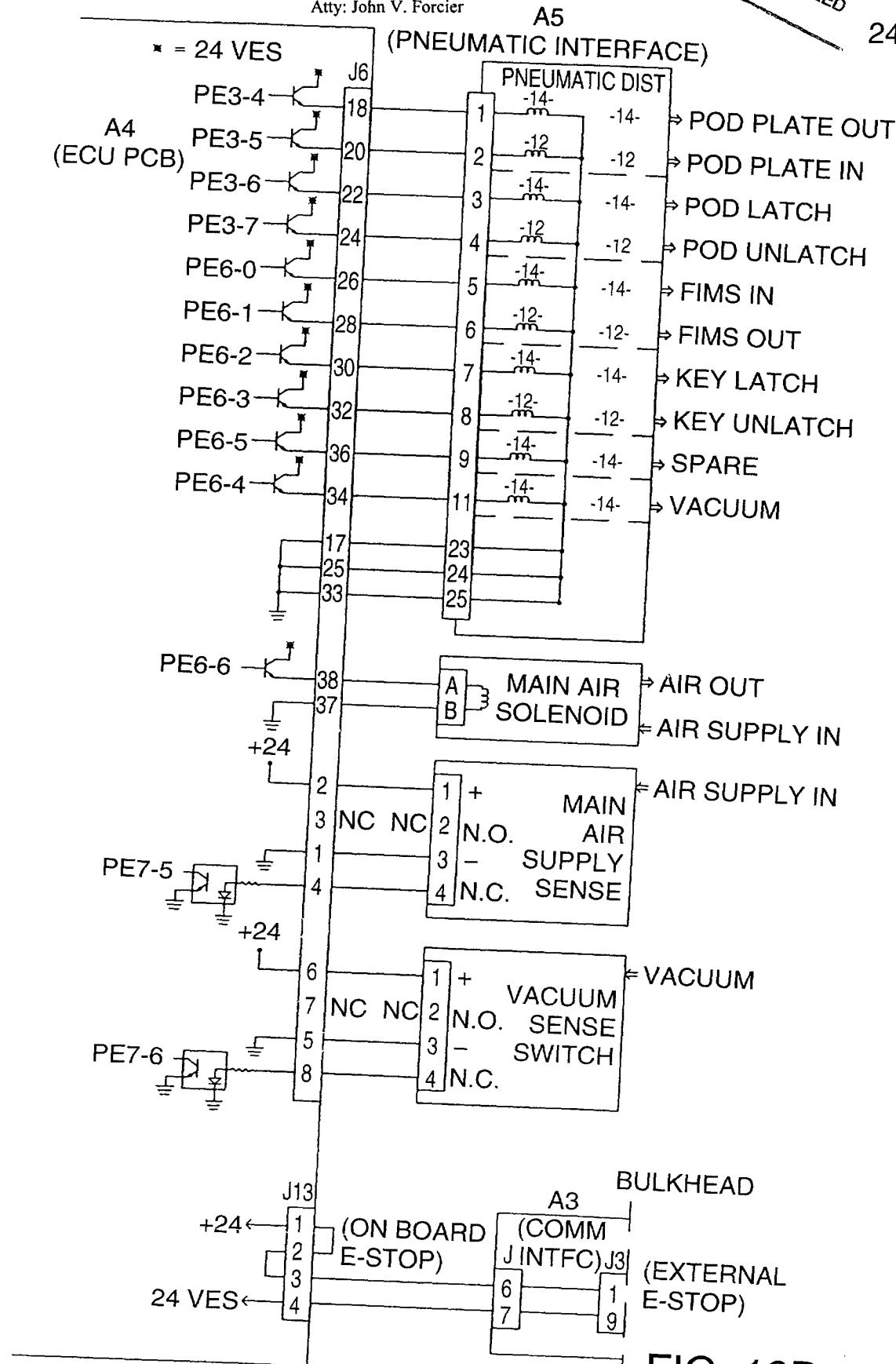


FIG. 10D

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POD PLATE / OBSTRUCTION / PINCH BAR

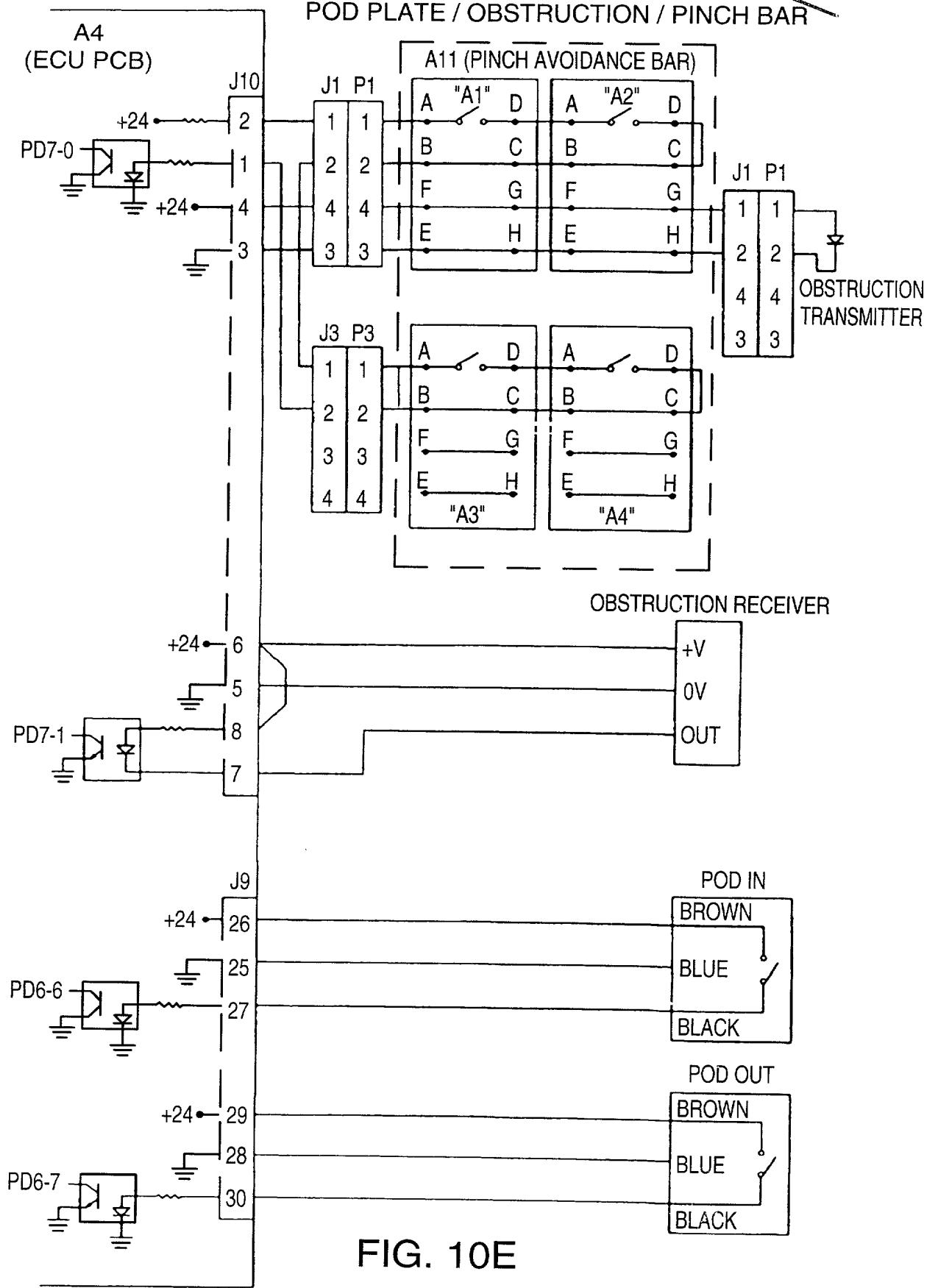
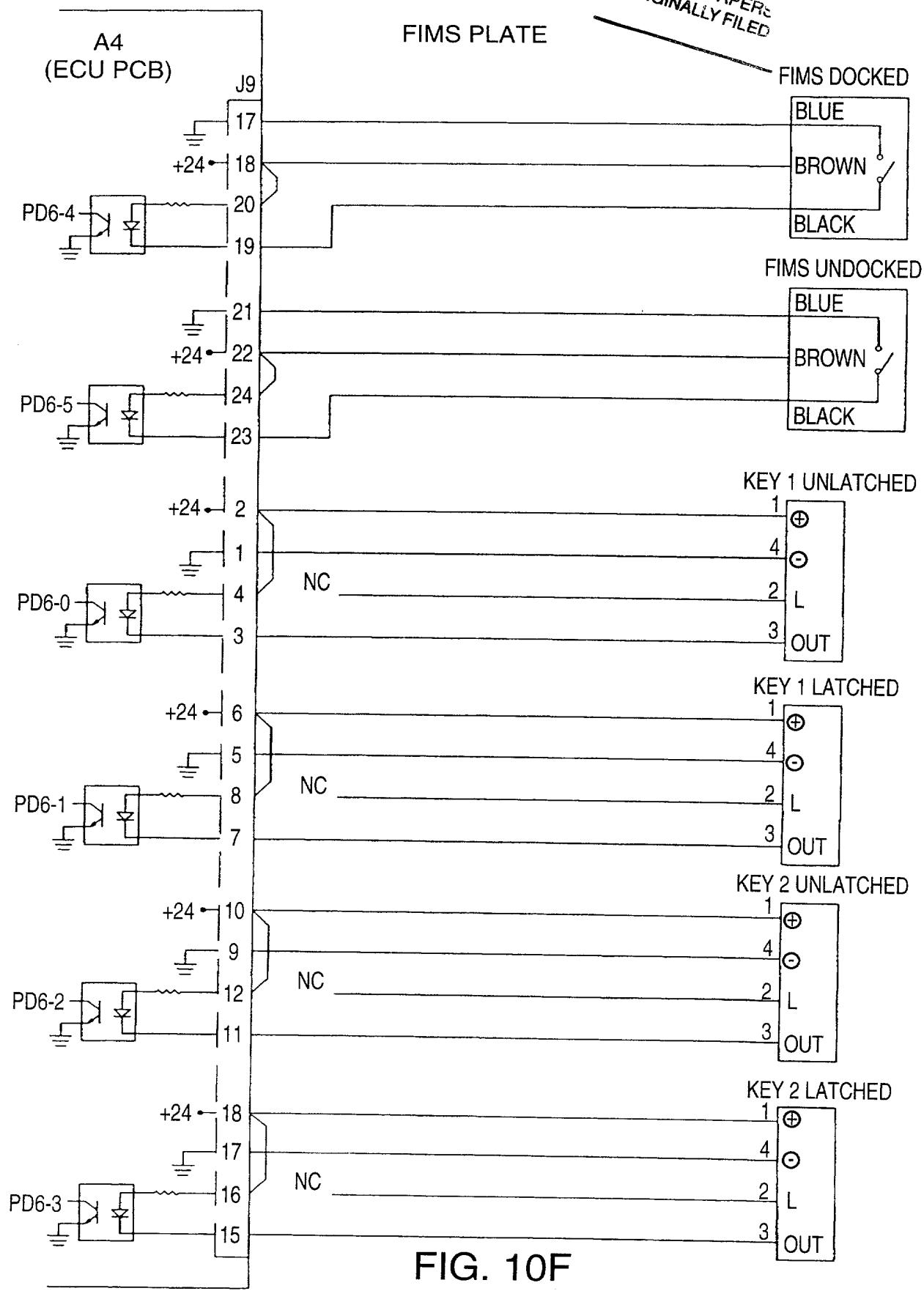


FIG. 10E

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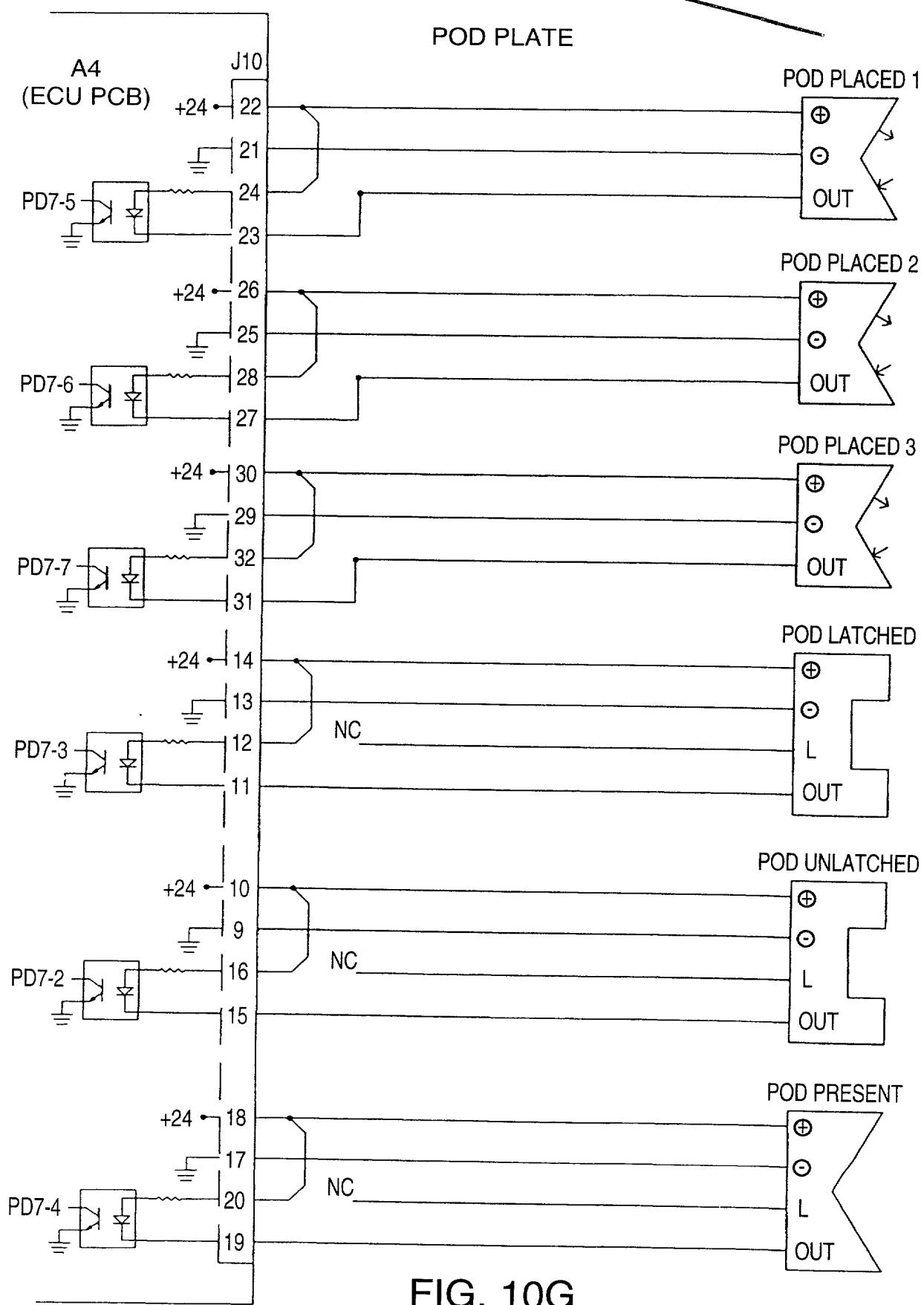


FIG. 10G

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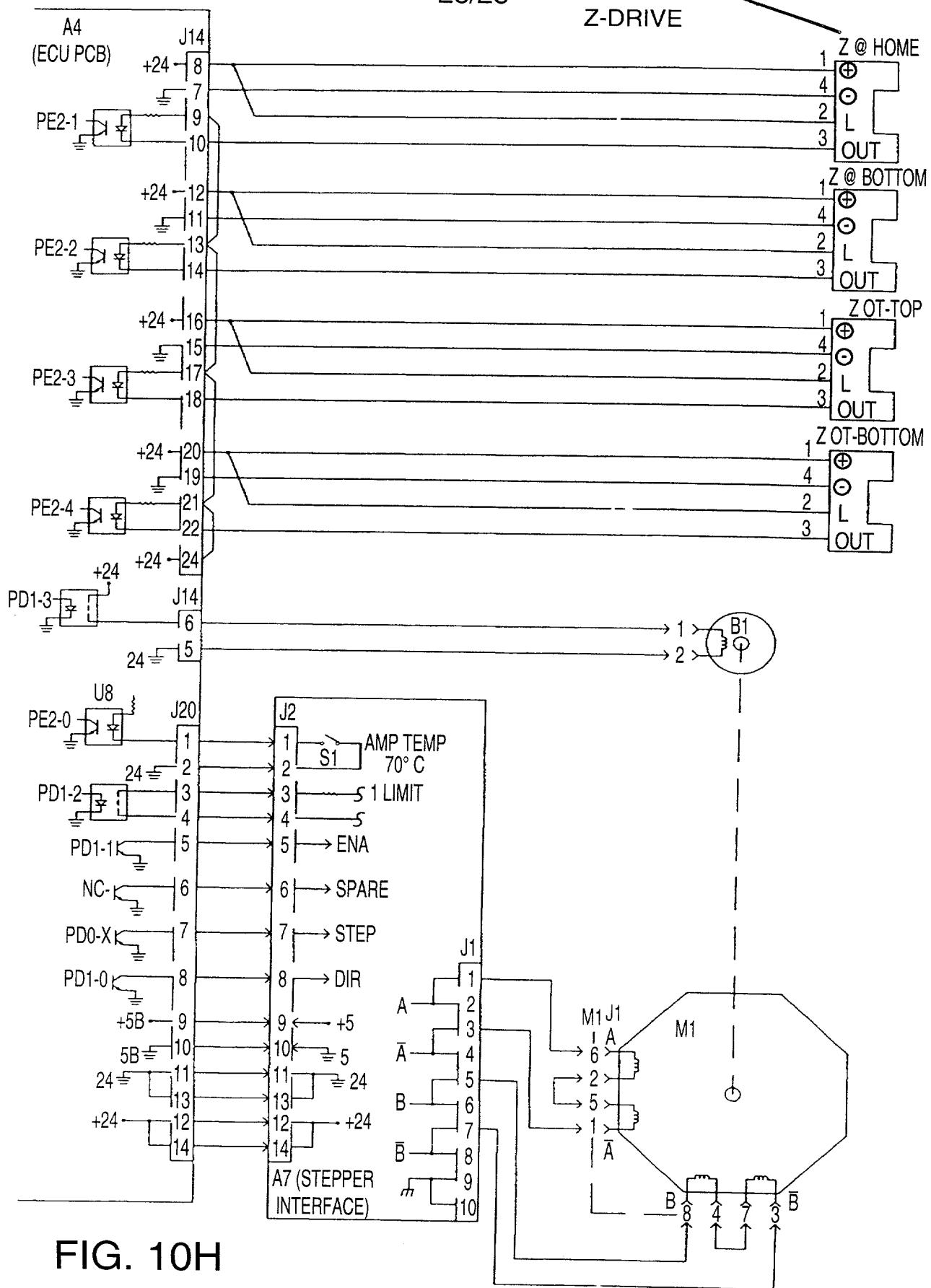


FIG. 10H